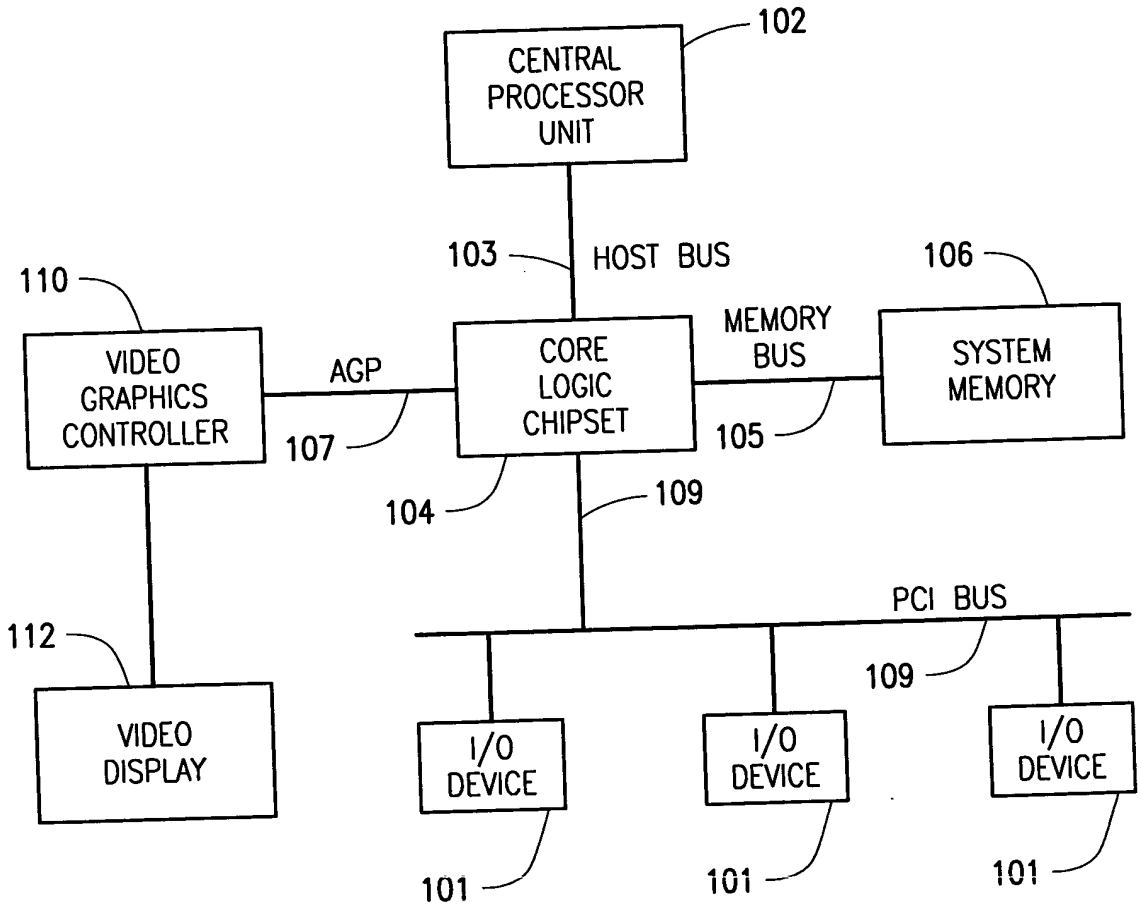


FIGURE 1
(PRIOR ART)

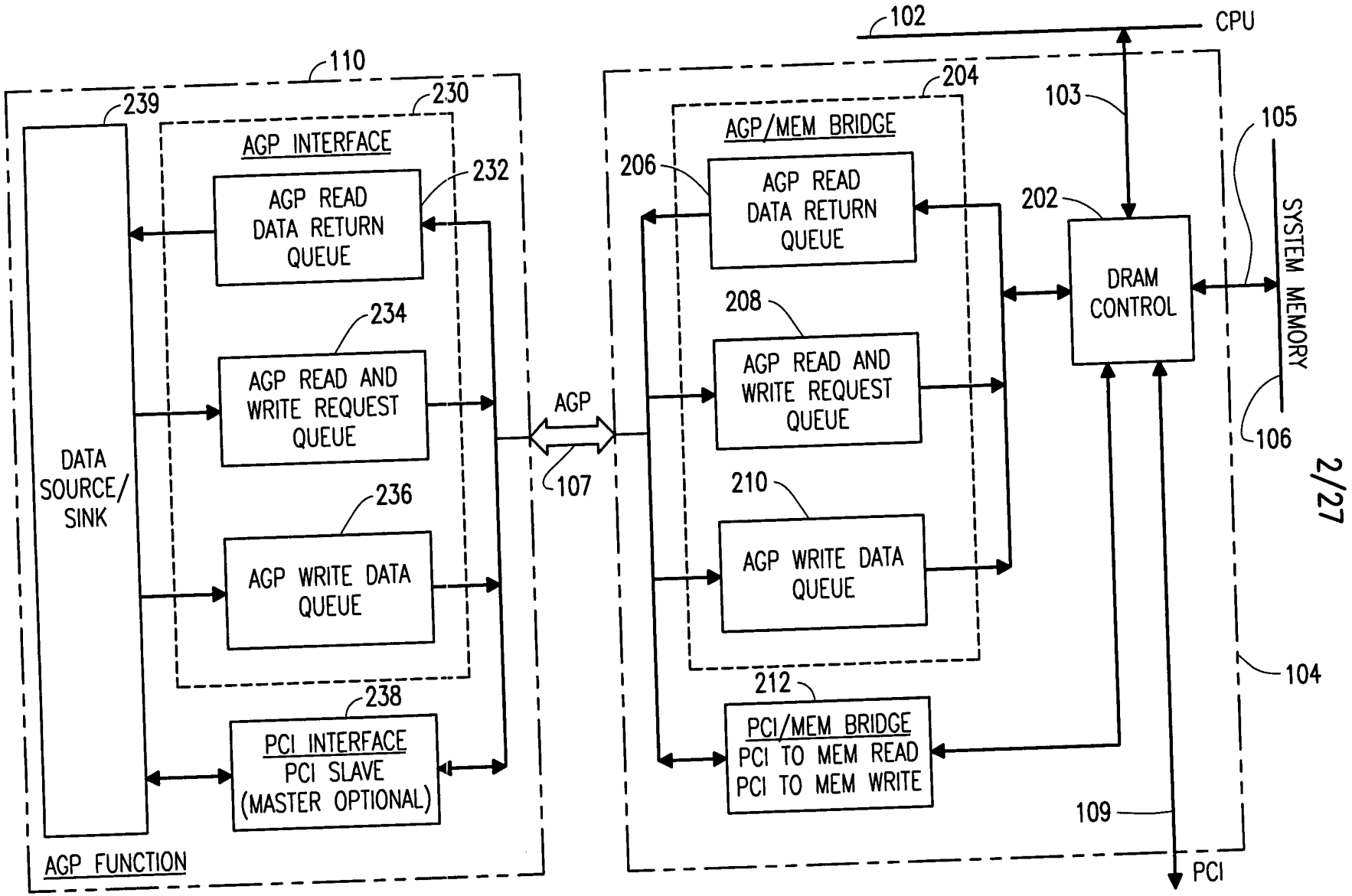


FIGURE 2
(PRIOR ART)

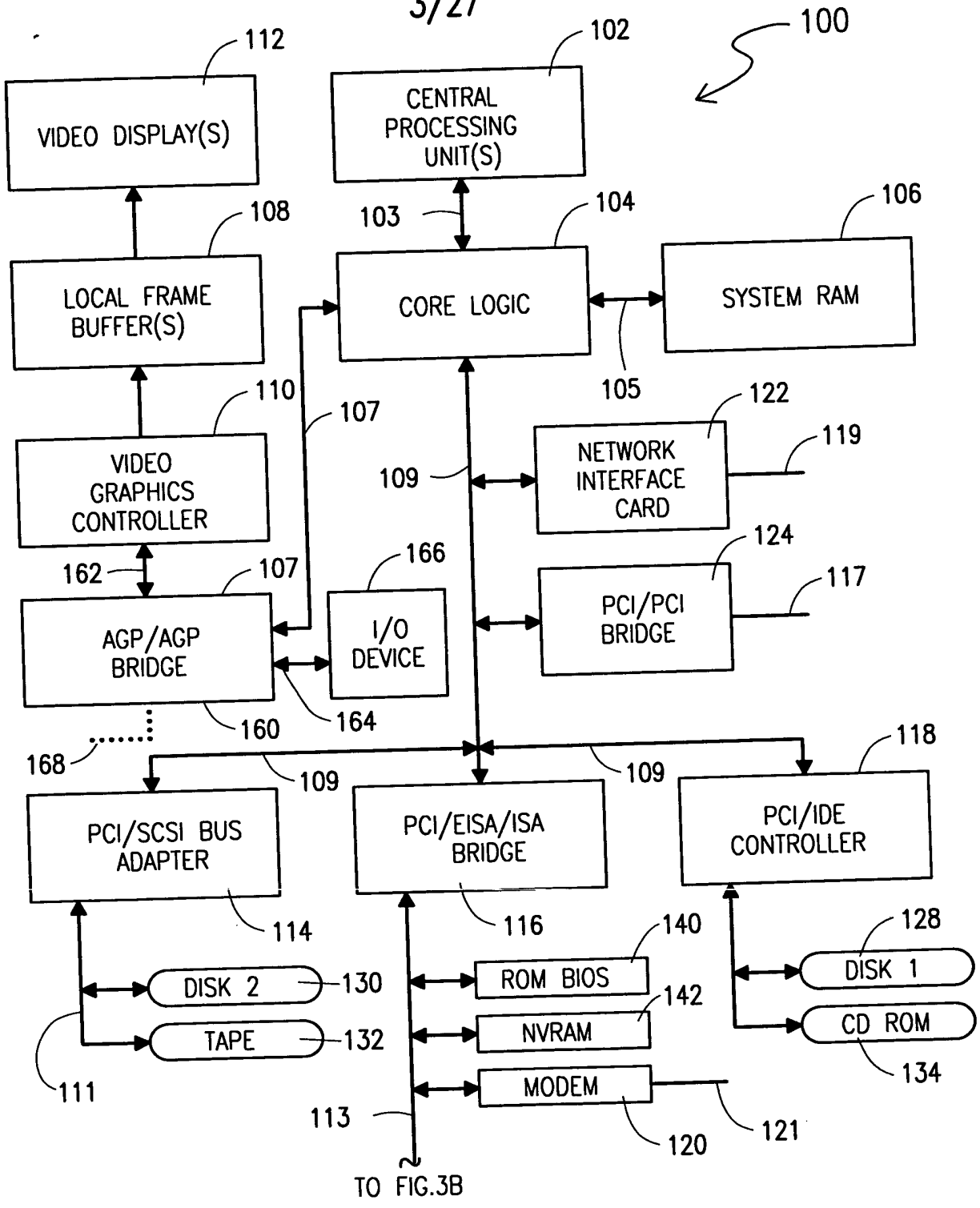

100
112
VIDEO DISPLAY(S)
102
CENTRAL PROCESSING UNIT(S)
103
104
106
108
LOCAL FRAME BUFFER(S)
CORE LOGIC
SYSTEM RAM
105
110
107
122
VIDEO GRAPHICS CONTROLLER
109
NETWORK INTERFACE CARD
119
124
162
107
166
117
AGP/AGP BRIDGE
I/O DEVICE
PCI/PCI BRIDGE
160
164
168
109
109
118
PCI/SCSI BUS ADAPTER
PCI/EISA/ISA BRIDGE
PCI/IDE CONTROLLER
114
116
140
128
DISK 2
130
ROM BIOS
DISK 1
142
TAPE
132
NVRAM
CD ROM
111
MODEM
134
113
120
121
TO FIG.3B

FIGURE 3A

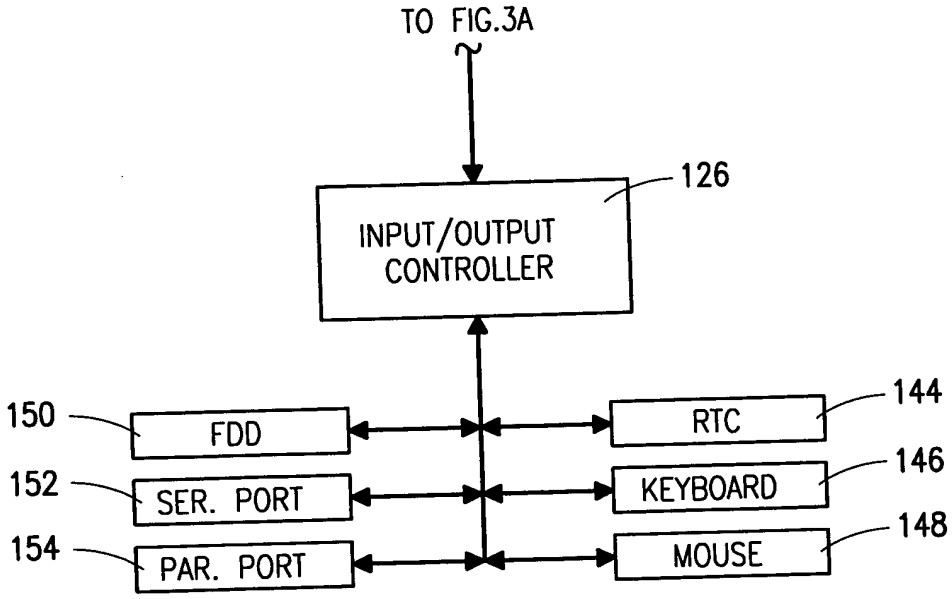

TO FIG.3A
126
INPUT/OUTPUT CONTROLLER
150
FDD
152
SER. PORT
154
PAR. PORT
144
RTC
146
KEYBOARD
148
MOUSE

FIGURE 3B

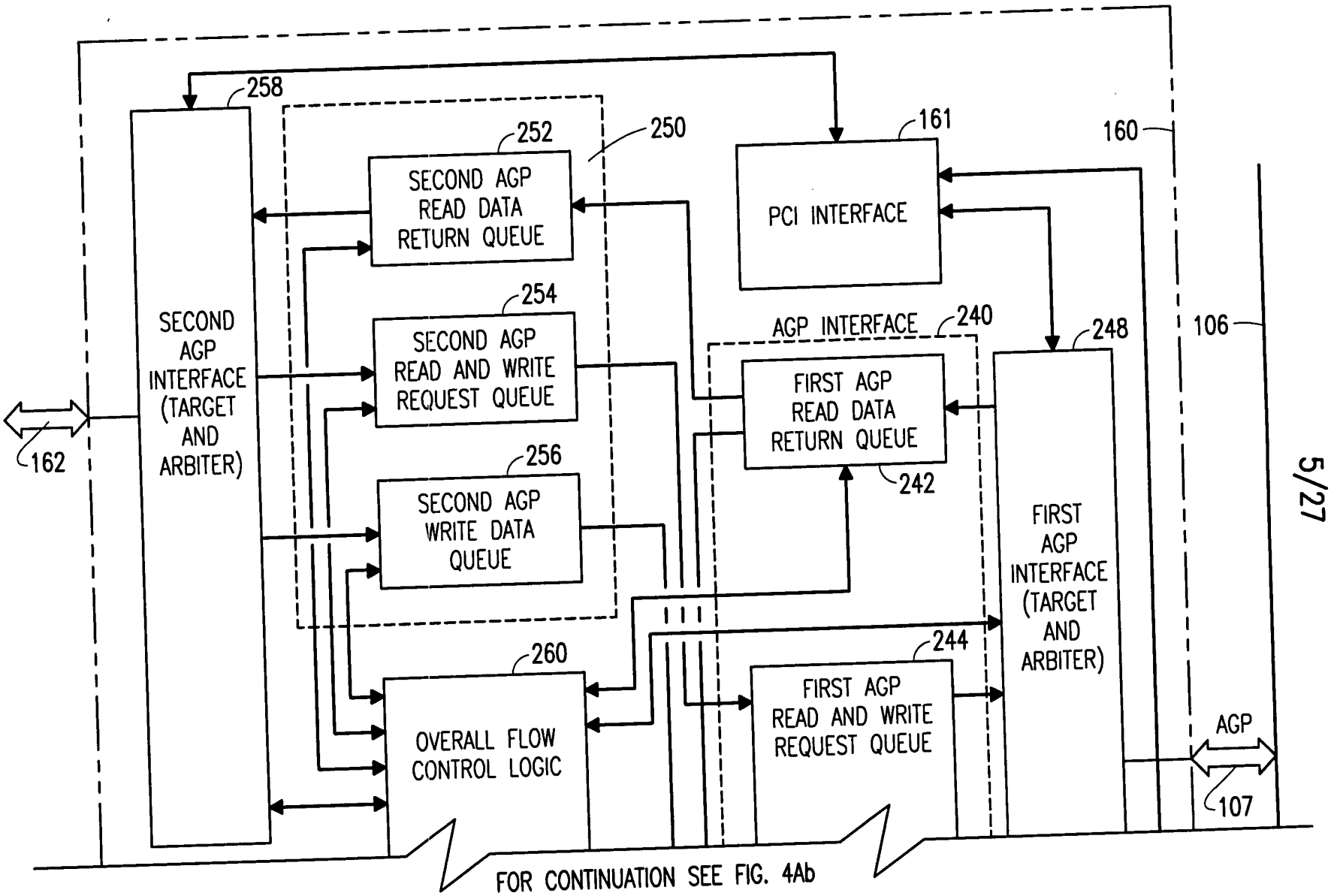

258
252
250
161
160
SECOND AGP READ DATA RETURN QUEUE
PCI INTERFACE
254
AGP INTERFACE
240
248
106
SECOND AGP INTERFACE (TARGET AND ARBITER)
SECOND AGP READ AND WRITE REQUEST QUEUE
FIRST AGP READ DATA RETURN QUEUE
162
256
242
SECOND AGP WRITE DATA QUEUE
FIRST AGP INTERFACE (TARGET AND ARBITER)
260
244
OVERALL FLOW CONTROL LOGIC
FIRST AGP READ AND WRITE REQUEST QUEUE
AGP
107
FOR CONTINUATION SEE FIG. 4Ab

FIGURE 4A

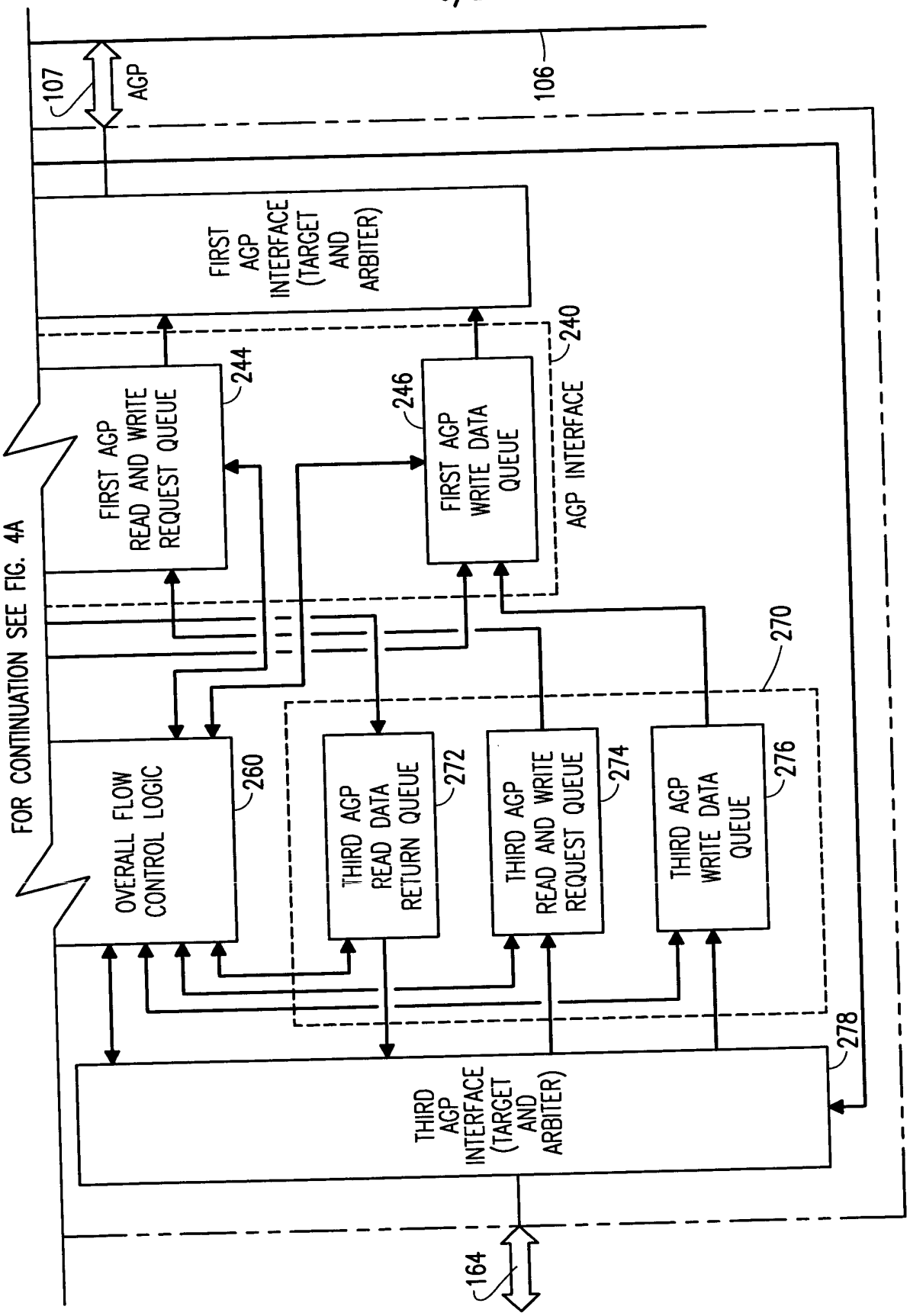

FOR CONTINUATION SEE FIG. 4A
107
AGP
106
FIRST AGP INTERFACE (TARGET AND ARBITER)
240
AGP INTERFACE
244
FIRST AGP READ AND WRITE REQUEST QUEUE
246
FIRST AGP WRITE DATA QUEUE
270
260
OVERALL FLOW CONTROL LOGIC
272
THIRD AGP READ DATA RETURN QUEUE
274
THIRD AGP READ AND WRITE REQUEST QUEUE
276
THIRD AGP WRITE DATA QUEUE
278
THIRD AGP INTERFACE (TARGET AND ARBITER)
164

FIGURE 4Ab

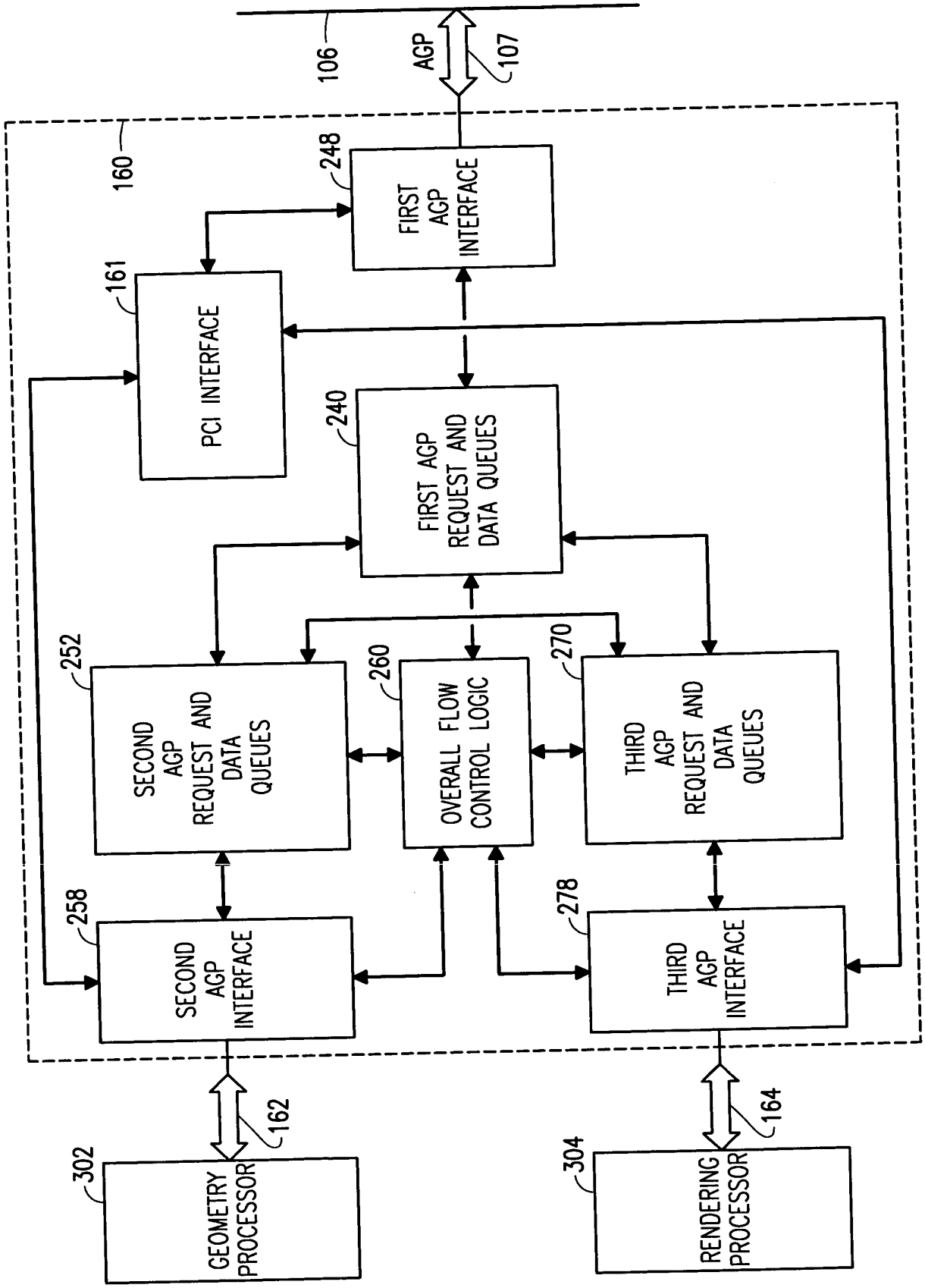

106
AGP
107
160
248
FIRST AGP INTERFACE
161
PCI INTERFACE
240
FIRST AGP REQUEST AND DATA QUEUES
252
SECOND AGP REQUEST AND DATA QUEUES
260
OVERALL FLOW CONTROL LOGIC
270
THIRD AGP REQUEST AND DATA QUEUES
258
SECOND AGP INTERFACE
278
THIRD AGP INTERFACE
162
164
302
GEOMETRY PROCESSOR
304
RENDERING PROCESSOR

FIGURE 4B

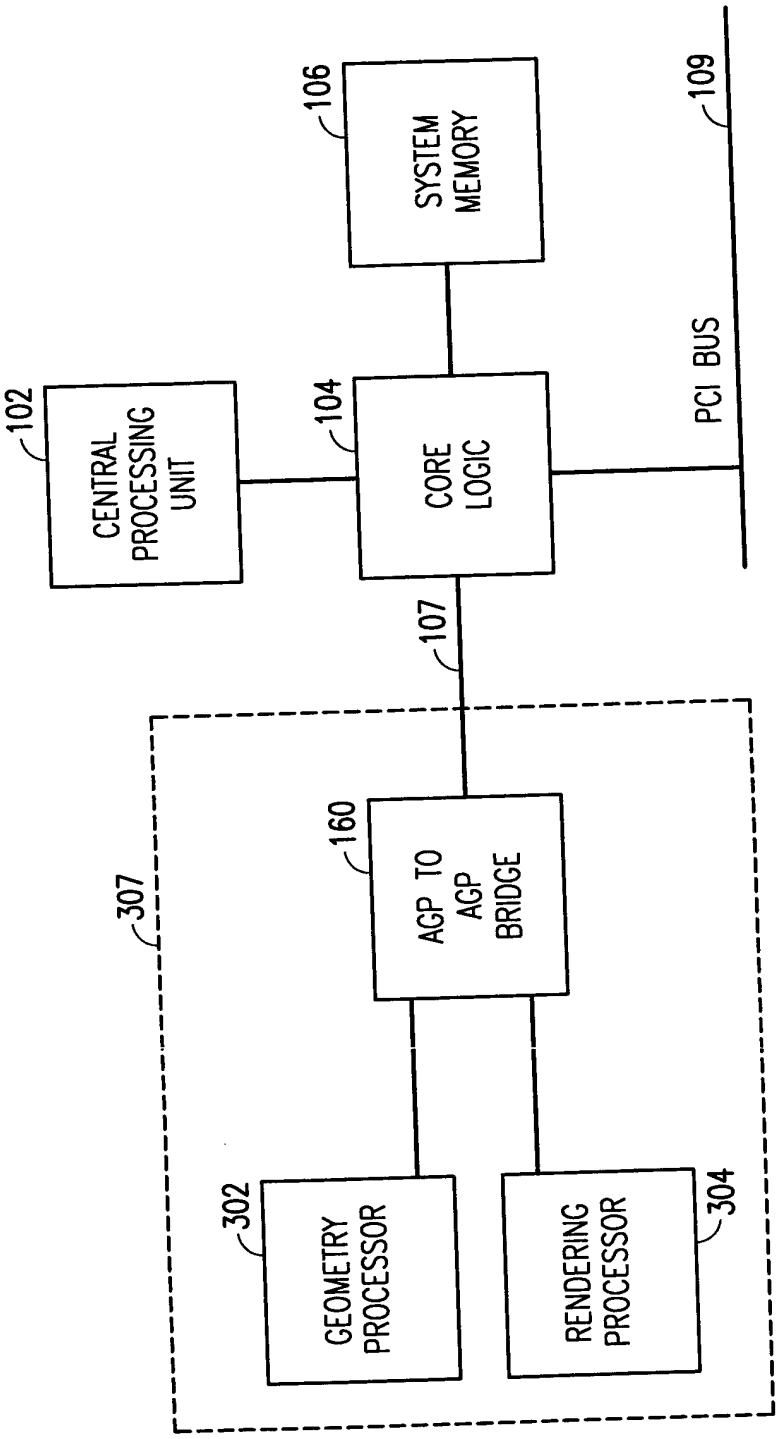

102
CENTRAL PROCESSING UNIT
104
CORE LOGIC
106
SYSTEM MEMORY
109
PCI BUS
107
307
160
AGP TO AGP BRIDGE
302
GEOMETRY PROCESSOR
304
RENDERING PROCESSOR

FIGURE 4C

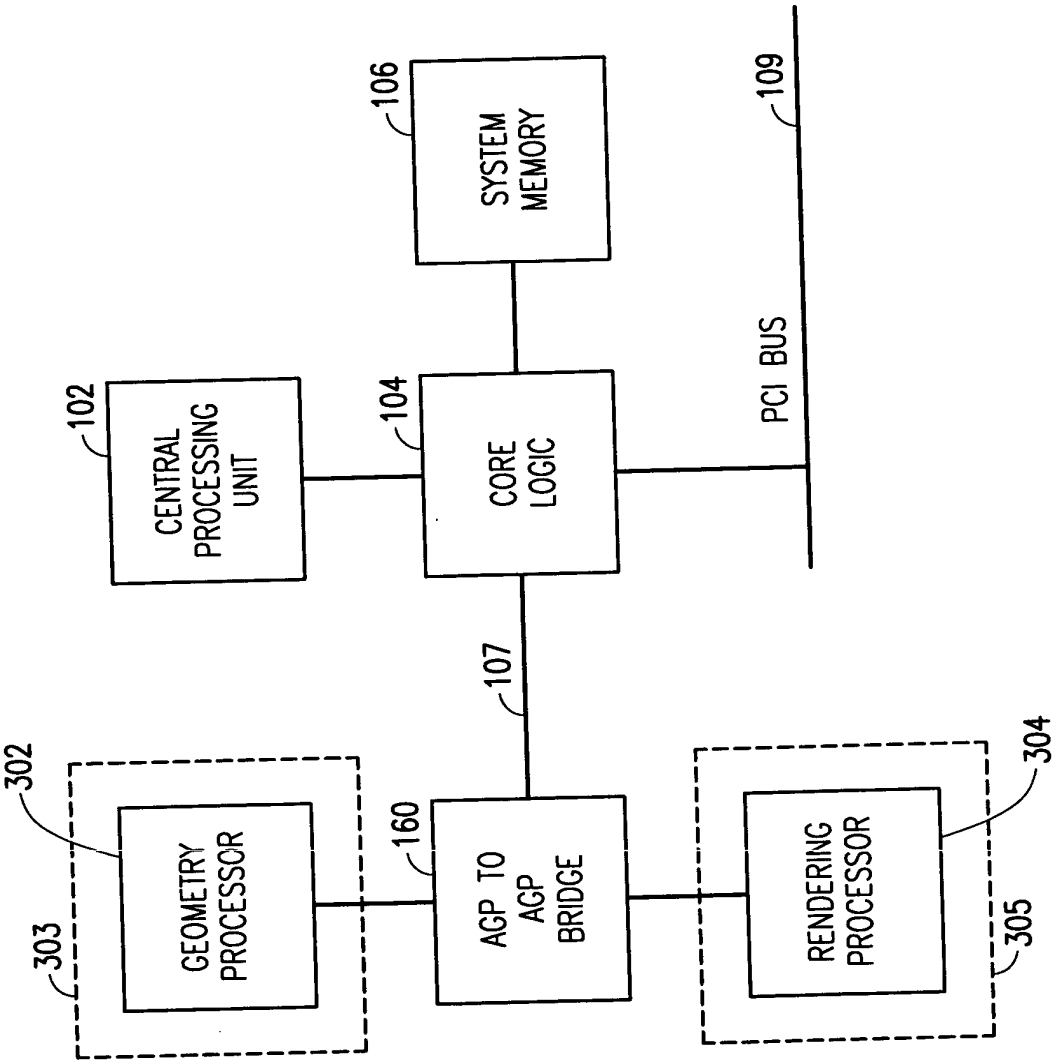

CENTRAL PROCESSING UNIT
102
CORE LOGIC
104
SYSTEM MEMORY
106
PCI BUS
109
107
AGP TO AGP BRIDGE
160
GEOMETRY PROCESSOR
302
303
RENDERING PROCESSOR
304
305

FIGURE 4D

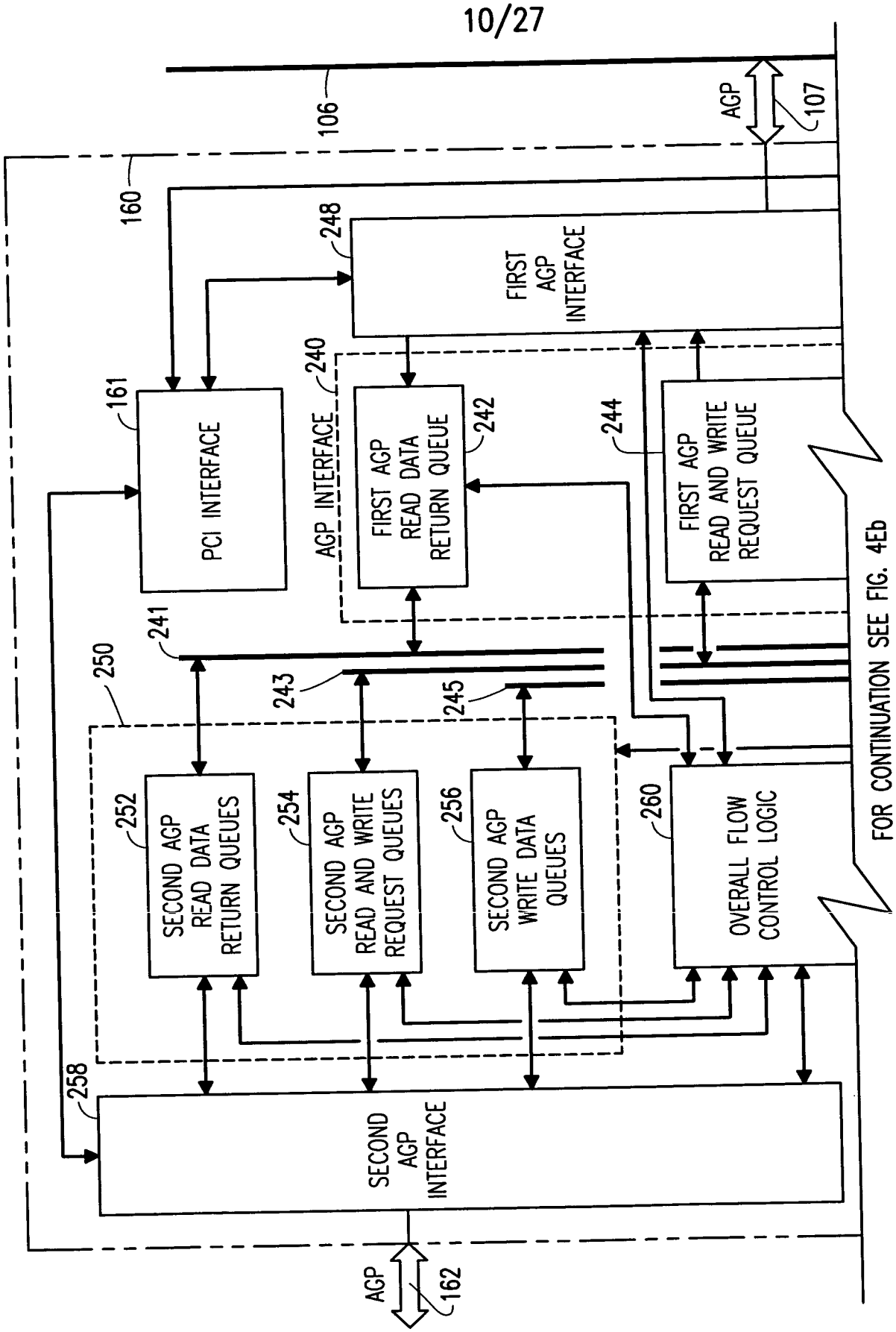

106
AGP
107
160
248
FIRST AGP INTERFACE
240
AGP INTERFACE
161
PCI INTERFACE
FIRST AGP READ DATA RETURN QUEUE
242
244
FIRST AGP READ AND WRITE REQUEST QUEUE
241
250
243
245
252
SECOND AGP READ DATA RETURN QUEUES
254
SECOND AGP READ AND WRITE REQUEST QUEUES
256
SECOND AGP WRITE DATA QUEUES
260
OVERALL FLOW CONTROL LOGIC
FOR CONTINUATION SEE FIG. 4Eb
258
SECOND AGP INTERFACE
AGP
162

FIGURE 4E

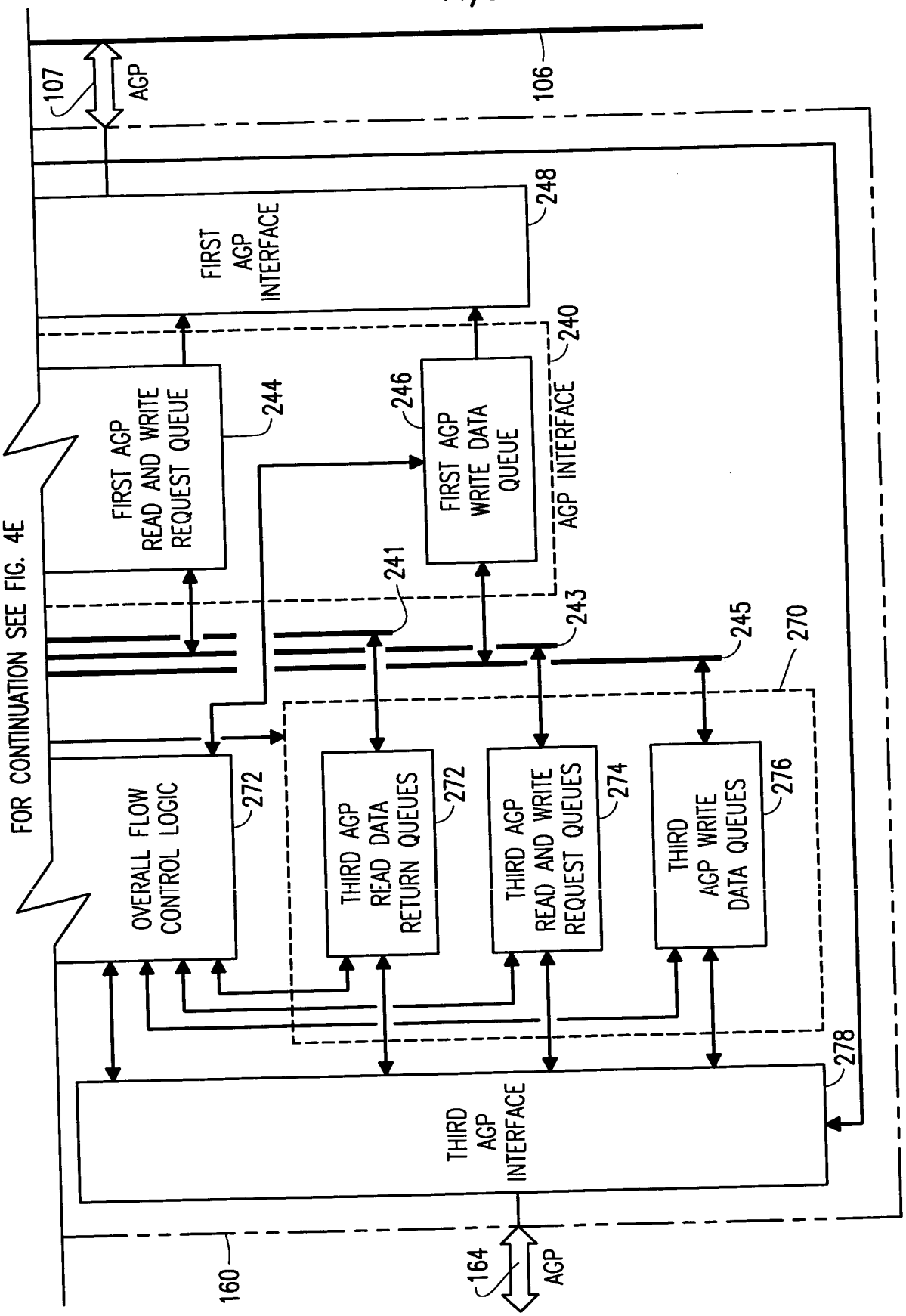

FOR CONTINUATION SEE FIG. 4E
107
AGP
106
FIRST AGP INTERFACE
248
240
FIRST AGP READ AND WRITE REQUEST QUEUE
244
246
FIRST AGP WRITE DATA QUEUE
AGP INTERFACE
241
243
245
270
OVERALL FLOW CONTROL LOGIC
272
THIRD AGP READ DATA RETURN QUEUES
272
THIRD AGP READ AND WRITE REQUEST QUEUES
274
THIRD AGP WRITE DATA QUEUES
276
278
THIRD AGP INTERFACE
160
164
AGP

FIGURE 4Eb

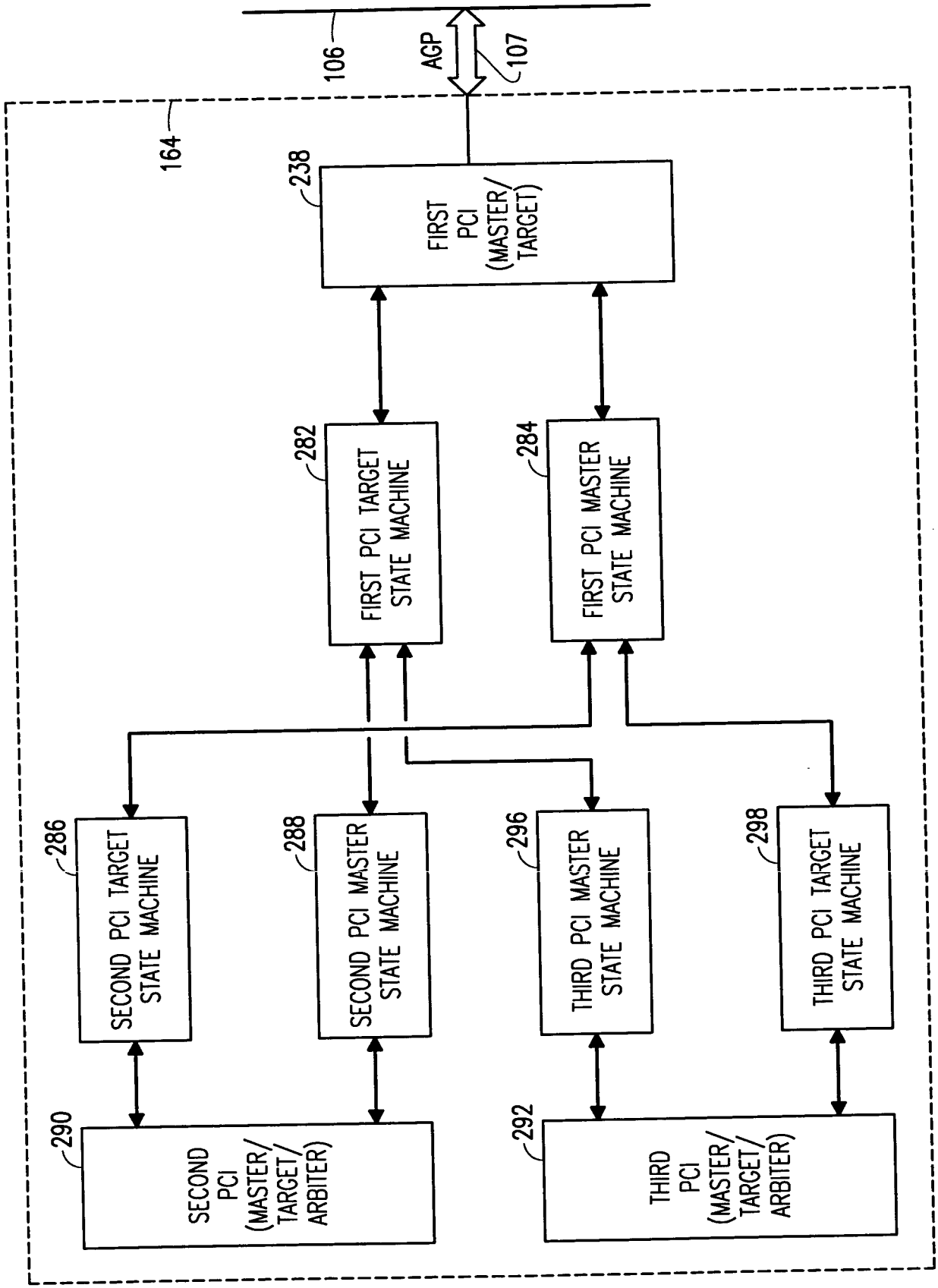

106
AGP
107
164
238
FIRST PCI (MASTER/ TARGET)
282
FIRST PCI TARGET STATE MACHINE
284
FIRST PCI MASTER STATE MACHINE
286
SECOND PCI TARGET STATE MACHINE
288
SECOND PCI MASTER STATE MACHINE
296
THIRD PCI MASTER STATE MACHINE
298
THIRD PCI TARGET STATE MACHINE
290
SECOND PCI (MASTER/ TARGET/ ARBITER)
292
THIRD PCI (MASTER/ TARGET/ ARBITER)

FIGURE 5

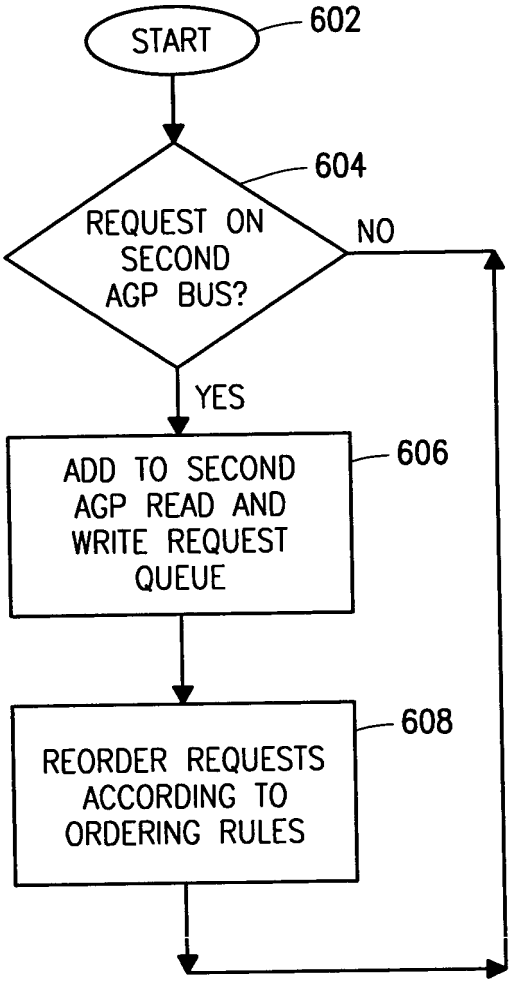


FIGURE 6

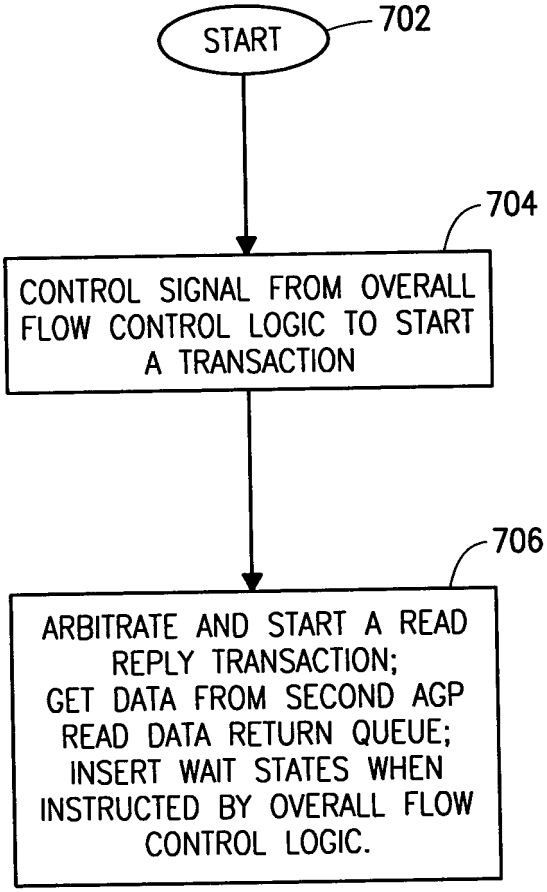

START
702
704
CONTROL SIGNAL FROM OVERALL FLOW CONTROL LOGIC TO START A TRANSACTION
706
ARBITRATE AND START A READ REPLY TRANSACTION; GET DATA FROM SECOND AGP READ DATA RETURN QUEUE; INSERT WAIT STATES WHEN INSTRUCTED BY OVERALL FLOW CONTROL LOGIC.

FIGURE 7

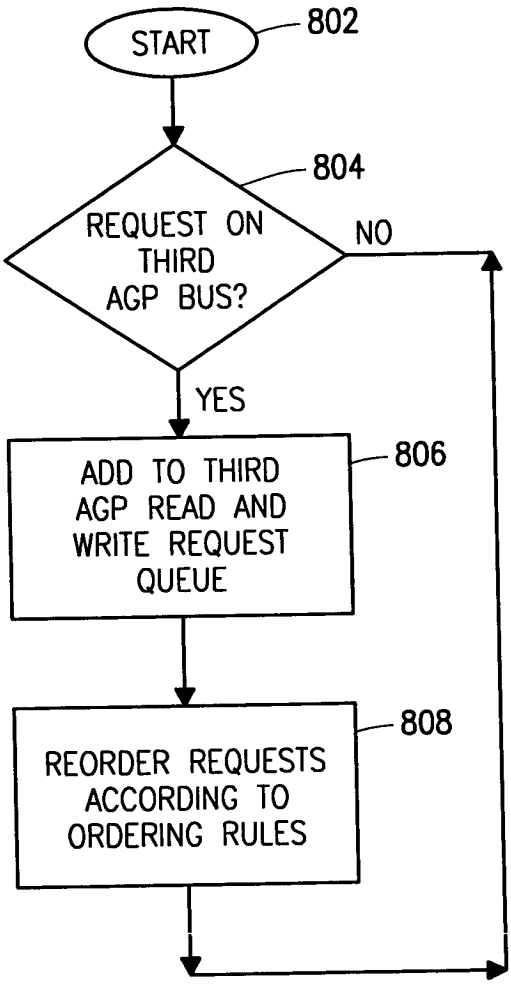


FIGURE 8

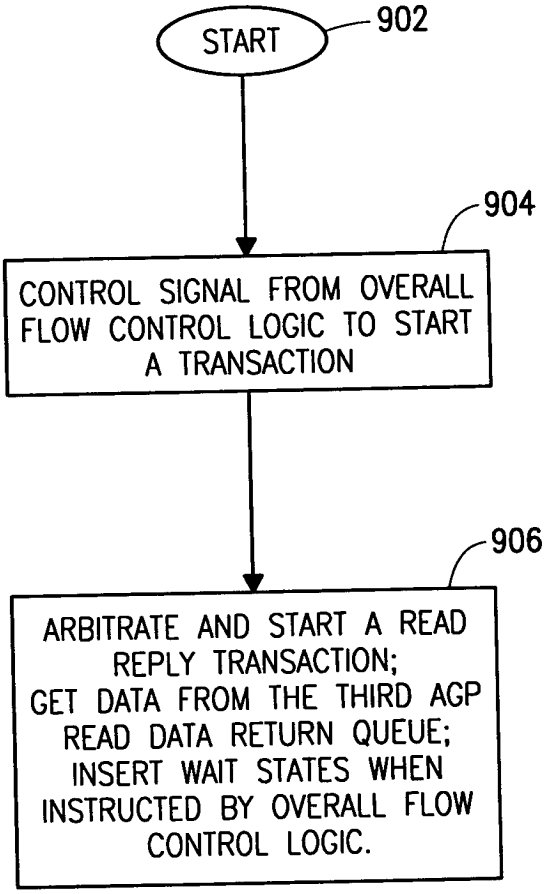

START
902
904
CONTROL SIGNAL FROM OVERALL FLOW CONTROL LOGIC TO START A TRANSACTION
906
ARBITRATE AND START A READ REPLY TRANSACTION; GET DATA FROM THE THIRD AGP READ DATA RETURN QUEUE; INSERT WAIT STATES WHEN INSTRUCTED BY OVERALL FLOW CONTROL LOGIC.

FIGURE 9

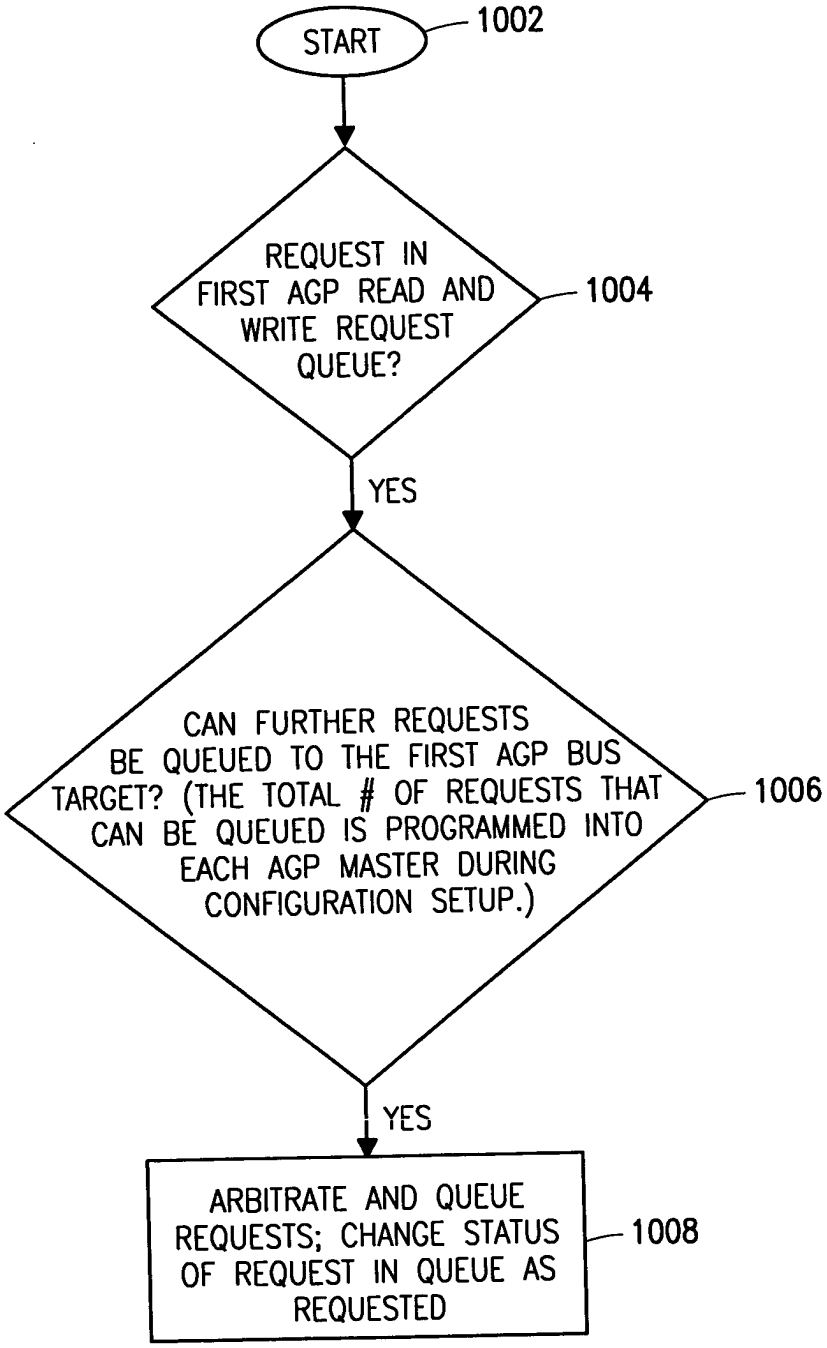

START
1002
REQUEST IN FIRST AGP READ AND WRITE REQUEST QUEUE?
1004
YES
CAN FURTHER REQUESTS BE QUEUED TO THE FIRST AGP BUS TARGET? (THE TOTAL # OF REQUESTS THAT CAN BE QUEUED IS PROGRAMMED INTO EACH AGP MASTER DURING CONFIGURATION SETUP.)
1006
YES
ARBITRATE AND QUEUE REQUESTS; CHANGE STATUS OF REQUEST IN QUEUE AS REQUESTED
1008

FIGURE 10

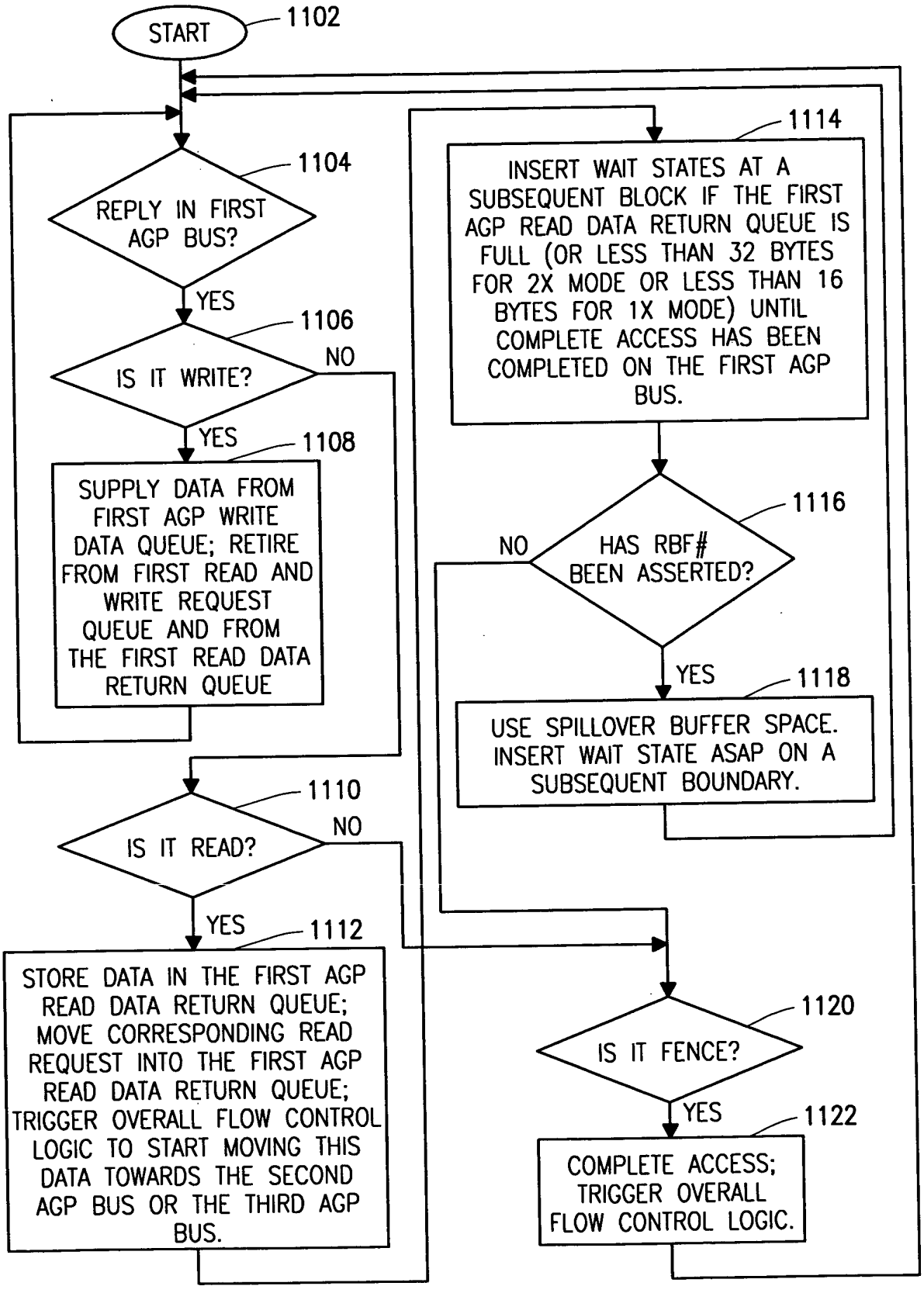

START
1102
1104
REPLY IN FIRST AGP BUS?
YES
1106
IS IT WRITE?
NO
YES
1108
SUPPLY DATA FROM FIRST AGP WRITE DATA QUEUE; RETIRE FROM FIRST READ AND WRITE REQUEST QUEUE AND FROM THE FIRST READ DATA RETURN QUEUE
1110
IS IT READ?
NO
YES
1112
STORE DATA IN THE FIRST AGP READ DATA RETURN QUEUE; MOVE CORRESPONDING READ REQUEST INTO THE FIRST AGP READ DATA RETURN QUEUE; TRIGGER OVERALL FLOW CONTROL LOGIC TO START MOVING THIS DATA TOWARDS THE SECOND AGP BUS OR THE THIRD AGP BUS.
1114
INSERT WAIT STATES AT A SUBSEQUENT BLOCK IF THE FIRST AGP READ DATA RETURN QUEUE IS FULL (OR LESS THAN 32 BYTES FOR 2X MODE OR LESS THAN 16 BYTES FOR 1X MODE) UNTIL COMPLETE ACCESS HAS BEEN COMPLETED ON THE FIRST AGP BUS.
1116
NO
HAS RBF# BEEN ASSERTED?
YES
1118
USE SPILLOVER BUFFER SPACE. INSERT WAIT STATE ASAP ON A SUBSEQUENT BOUNDARY.
1120
IS IT FENCE?
YES
1122
COMPLETE ACCESS; TRIGGER OVERALL FLOW CONTROL LOGIC.

FIGURE 11

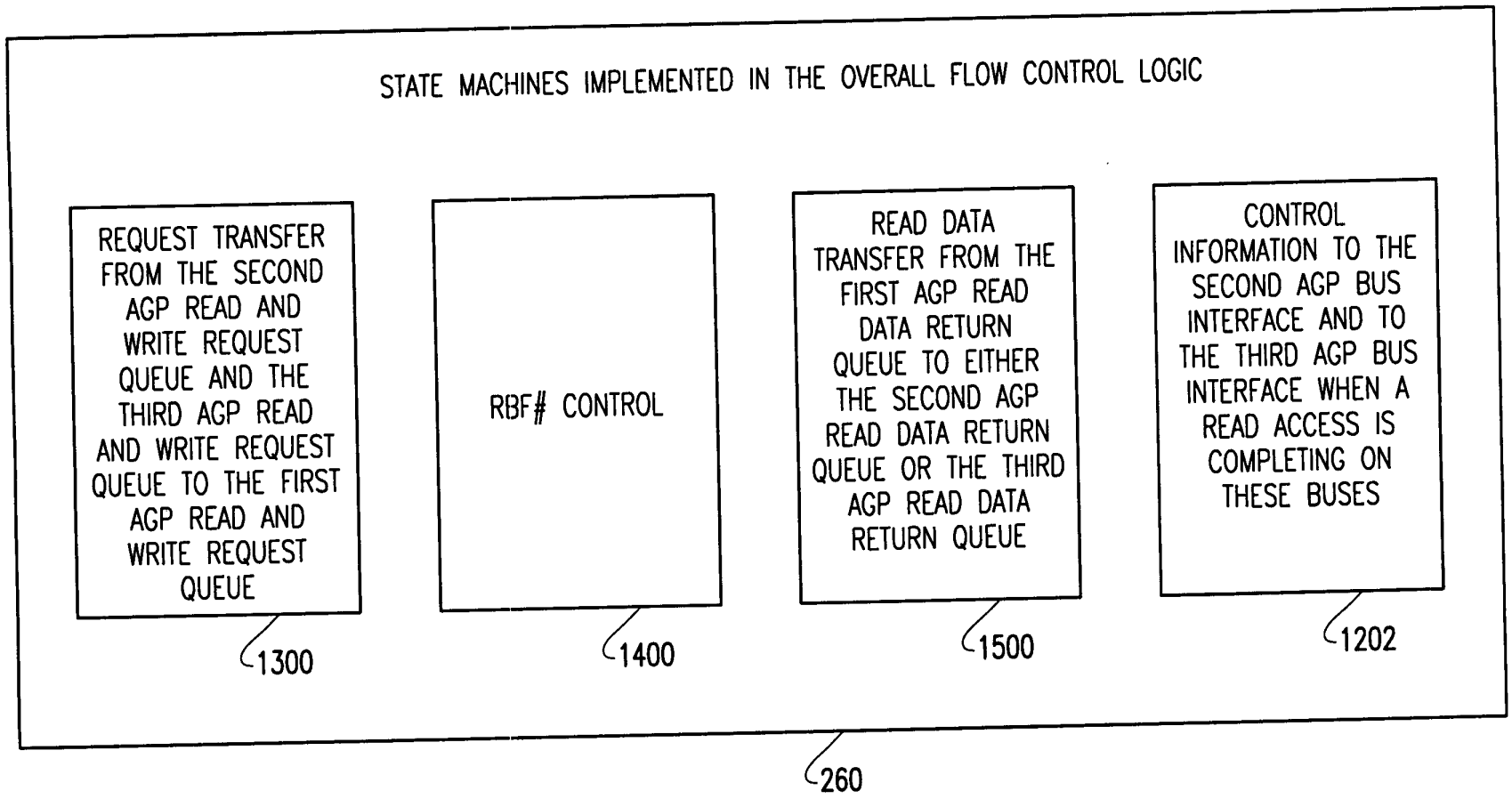
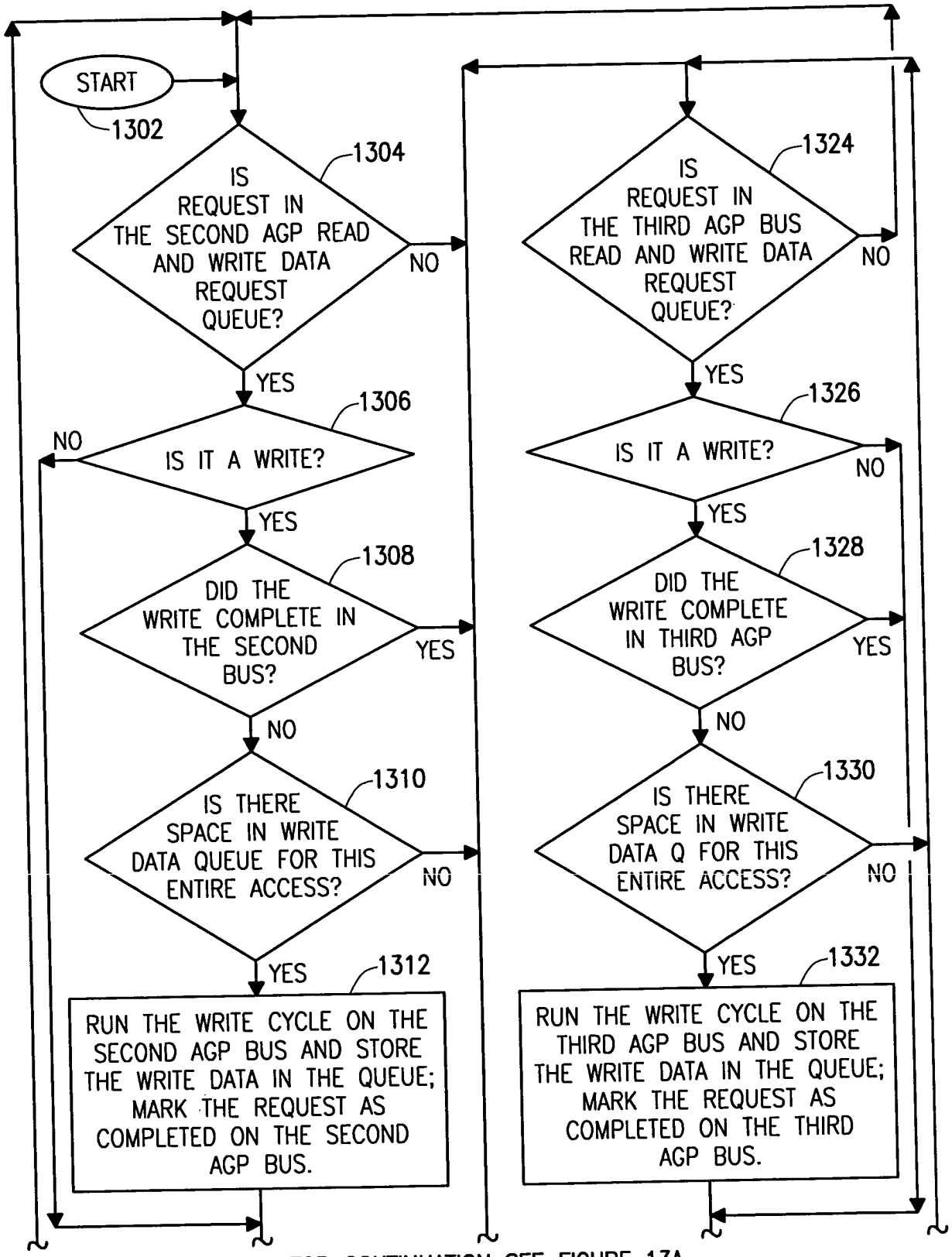

STATE MACHINES IMPLEMENTED IN THE OVERALL FLOW CONTROL LOGIC
REQUEST TRANSFER FROM THE SECOND AGP READ AND WRITE REQUEST QUEUE AND THE THIRD AGP READ AND WRITE REQUEST QUEUE TO THE FIRST AGP READ AND WRITE REQUEST QUEUE
1300
RBF# CONTROL
1400
READ DATA TRANSFER FROM THE FIRST AGP READ DATA RETURN QUEUE TO EITHER THE SECOND AGP READ DATA RETURN QUEUE OR THE THIRD AGP READ DATA RETURN QUEUE
1500
CONTROL INFORMATION TO THE SECOND AGP BUS INTERFACE AND TO THE THIRD AGP BUS INTERFACE WHEN A READ ACCESS IS COMPLETING ON THESE BUSES
1202
260

FIGURE 12


START
1302
1304
IS REQUEST IN THE SECOND AGP READ AND WRITE DATA REQUEST QUEUE?
NO
YES
1306
IS IT A WRITE?
NO
YES
1308
DID THE WRITE COMPLETE IN THE SECOND BUS?
YES
NO
1310
IS THERE SPACE IN WRITE DATA QUEUE FOR THIS ENTIRE ACCESS?
NO
YES
1312
RUN THE WRITE CYCLE ON THE SECOND AGP BUS AND STORE THE WRITE DATA IN THE QUEUE; MARK THE REQUEST AS COMPLETED ON THE SECOND AGP BUS.
1324
IS REQUEST IN THE THIRD AGP BUS READ AND WRITE DATA REQUEST QUEUE?
NO
YES
1326
IS IT A WRITE?
NO
YES
1328
DID THE WRITE COMPLETE IN THIRD AGP BUS?
YES
NO
1330
IS THERE SPACE IN WRITE DATA Q FOR THIS ENTIRE ACCESS?
NO
YES
1332
RUN THE WRITE CYCLE ON THE THIRD AGP BUS AND STORE THE WRITE DATA IN THE QUEUE; MARK THE REQUEST AS COMPLETED ON THE THIRD AGP BUS.

FOR CONTINUATION SEE FIGURE 13A

FIGURE 13

FOR CONTINUATION SEE FIGURE 13

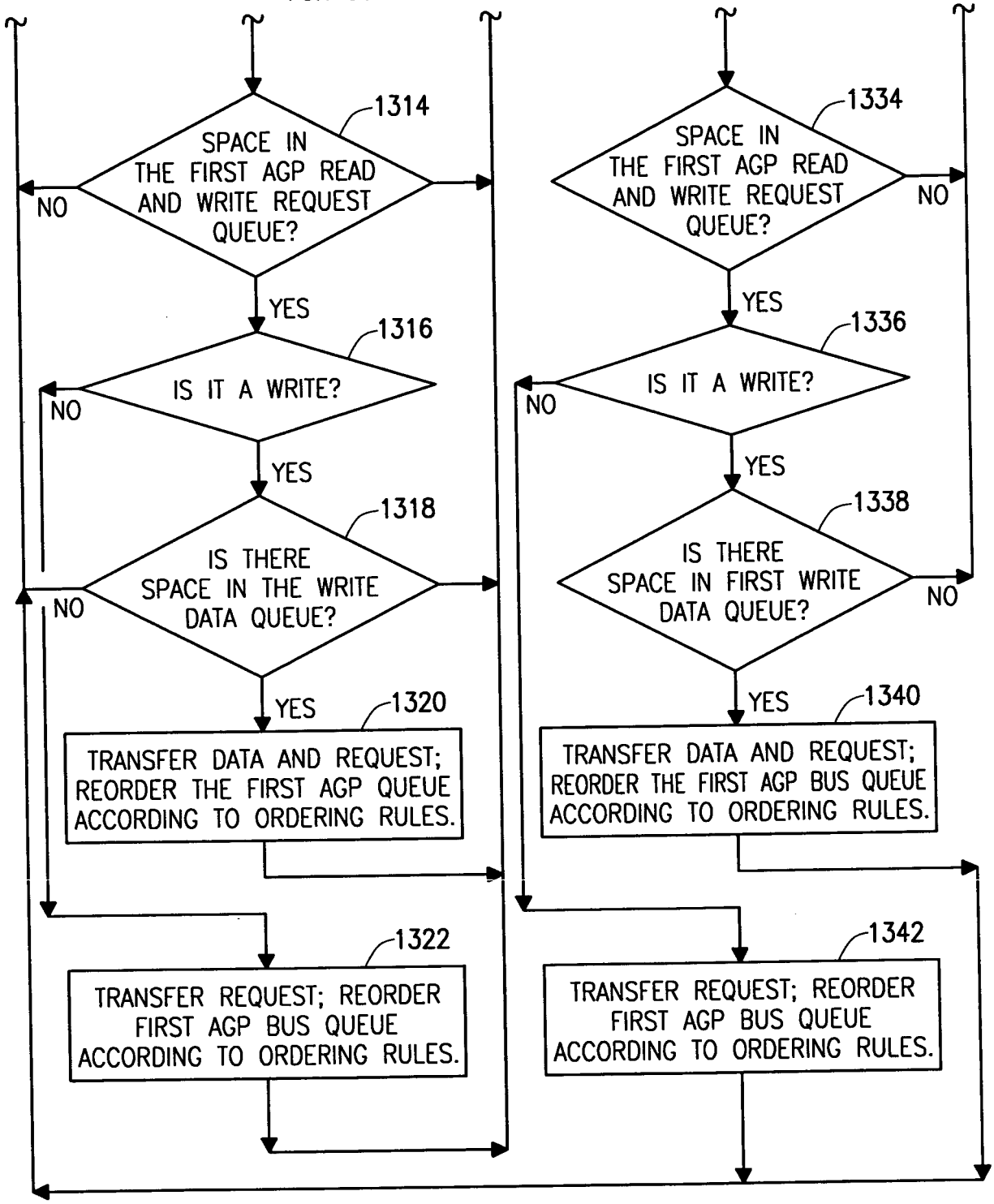
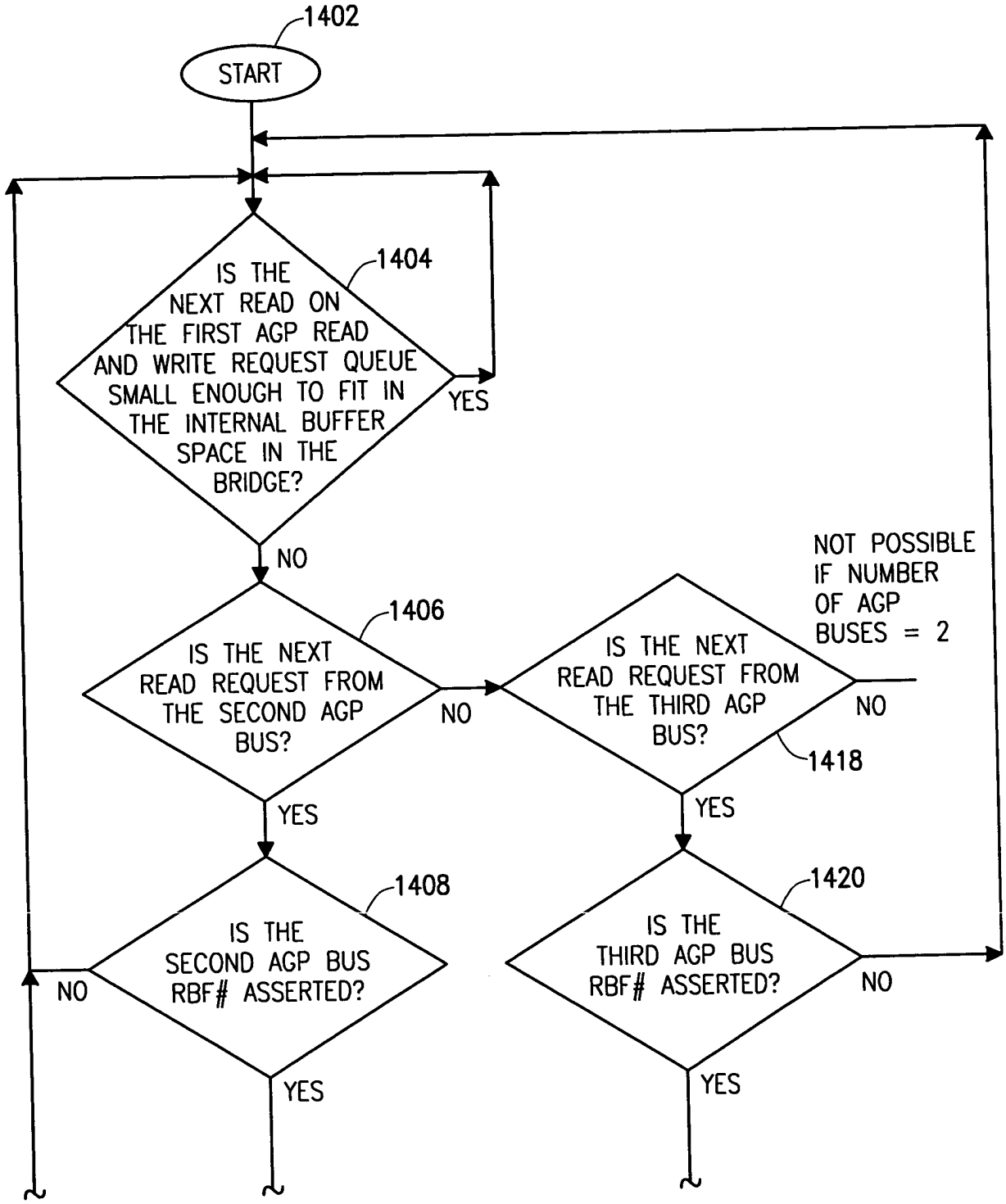


FIGURE 13A



FOR CONTINUATION SEE FIGURE 14A

FIGURE 14

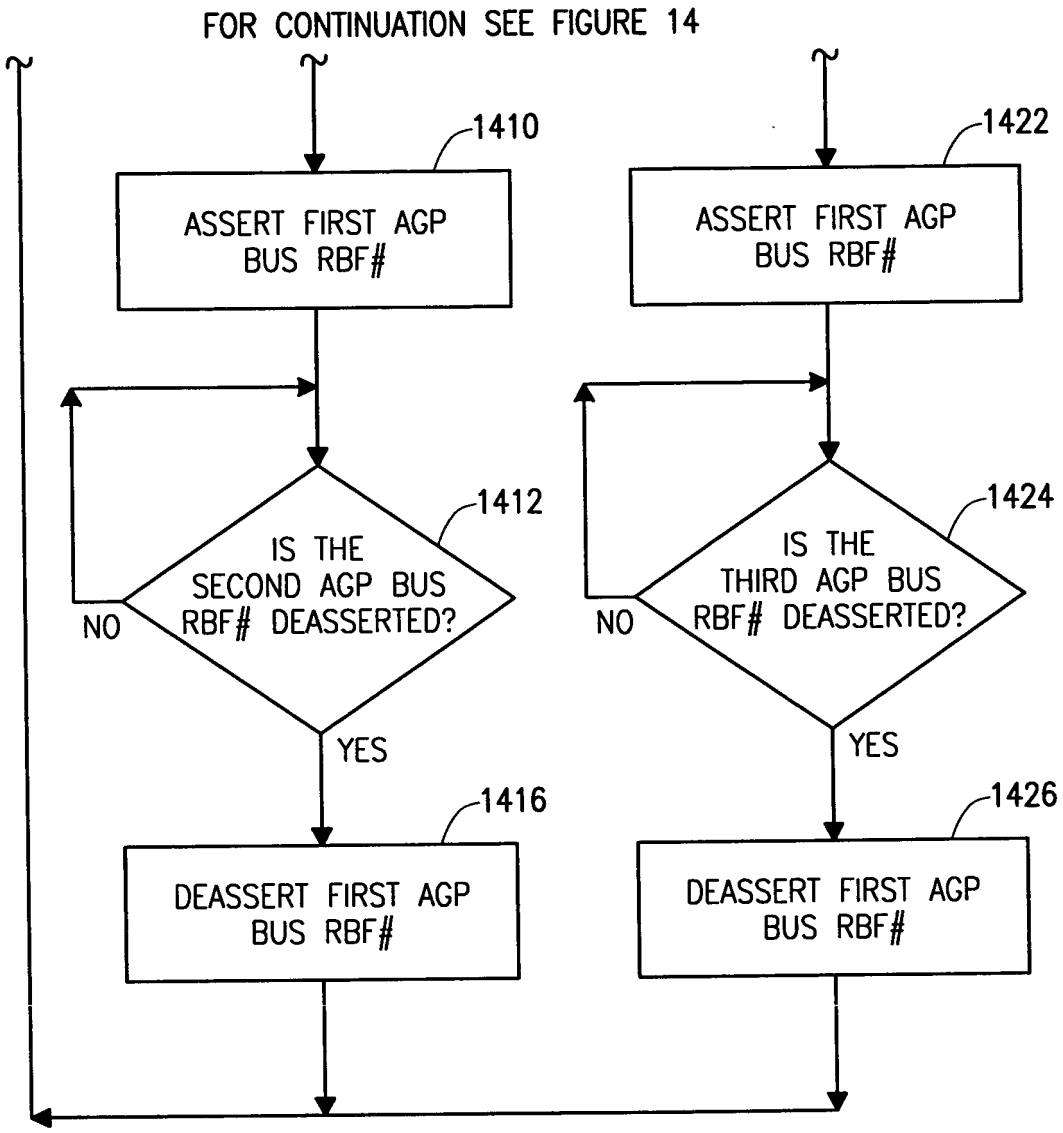

FOR CONTINUATION SEE FIGURE 14
1410
ASSERT FIRST AGP BUS RBF#
1412
IS THE SECOND AGP BUS RBF# DEASSERTED?
NO
YES
1416
DEASSERT FIRST AGP BUS RBF#
1422
ASSERT FIRST AGP BUS RBF#
1424
IS THE THIRD AGP BUS RBF# DEASSERTED?
NO
YES
1426
DEASSERT FIRST AGP BUS RBF#

FIGURE 14A

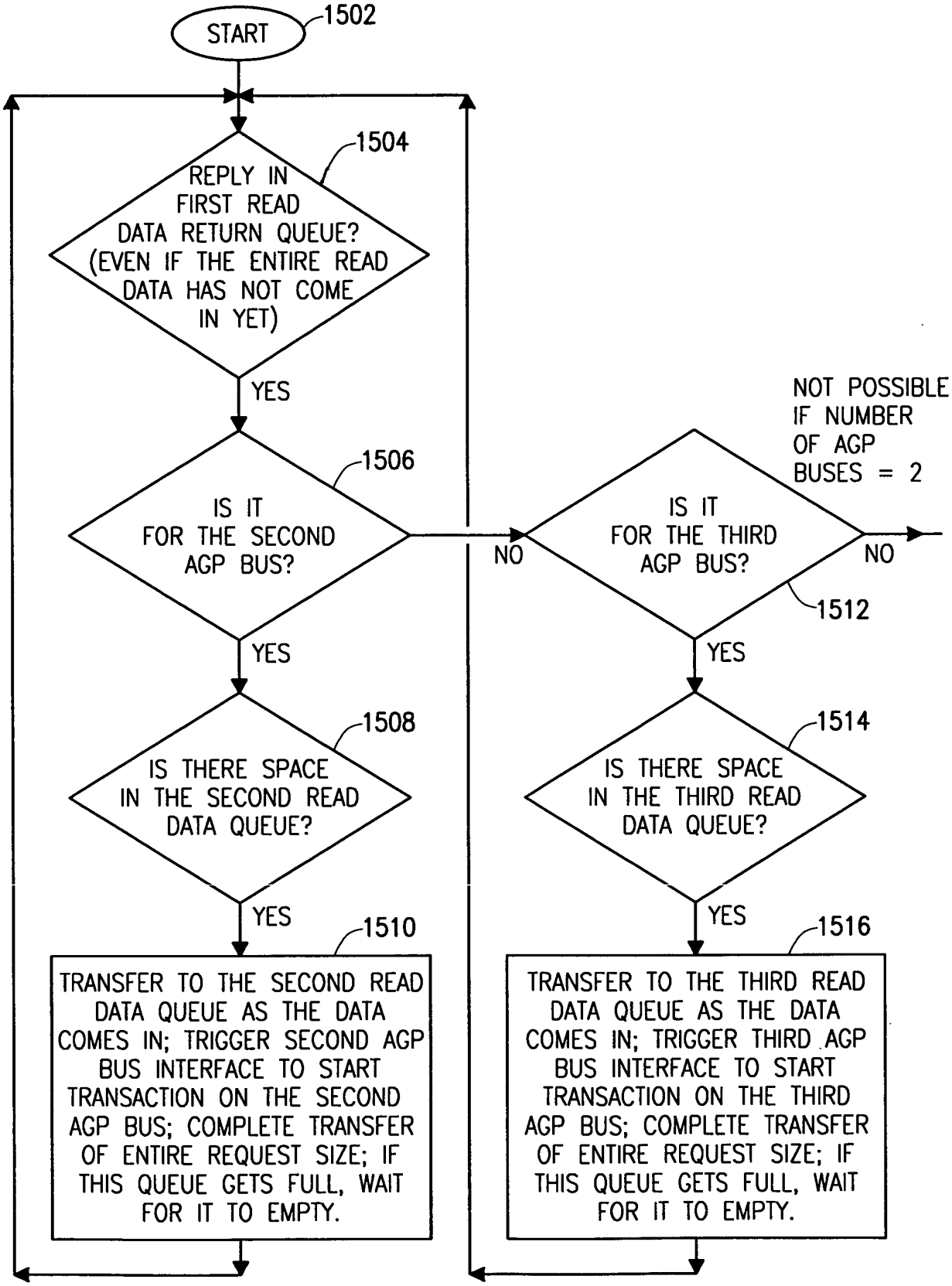

START
1502
1504
REPLY IN FIRST READ DATA RETURN QUEUE? (EVEN IF THE ENTIRE READ DATA HAS NOT COME IN YET)
YES
1506
IS IT FOR THE SECOND AGP BUS?
NO
NOT POSSIBLE IF NUMBER OF AGP BUSES = 2
IS IT FOR THE THIRD AGP BUS?
NO
1512
YES
YES
1508
IS THERE SPACE IN THE SECOND READ DATA QUEUE?
1514
IS THERE SPACE IN THE THIRD READ DATA QUEUE?
YES
YES
1510
TRANSFER TO THE SECOND READ DATA QUEUE AS THE DATA COMES IN; TRIGGER SECOND AGP BUS INTERFACE TO START TRANSACTION ON THE SECOND AGP BUS; COMPLETE TRANSFER OF ENTIRE REQUEST SIZE; IF THIS QUEUE GETS FULL, WAIT FOR IT TO EMPTY.
1516
TRANSFER TO THE THIRD READ DATA QUEUE AS THE DATA COMES IN; TRIGGER THIRD AGP BUS INTERFACE TO START TRANSACTION ON THE THIRD AGP BUS; COMPLETE TRANSFER OF ENTIRE REQUEST SIZE; IF THIS QUEUE GETS FULL, WAIT FOR IT TO EMPTY.

FIGURE 15

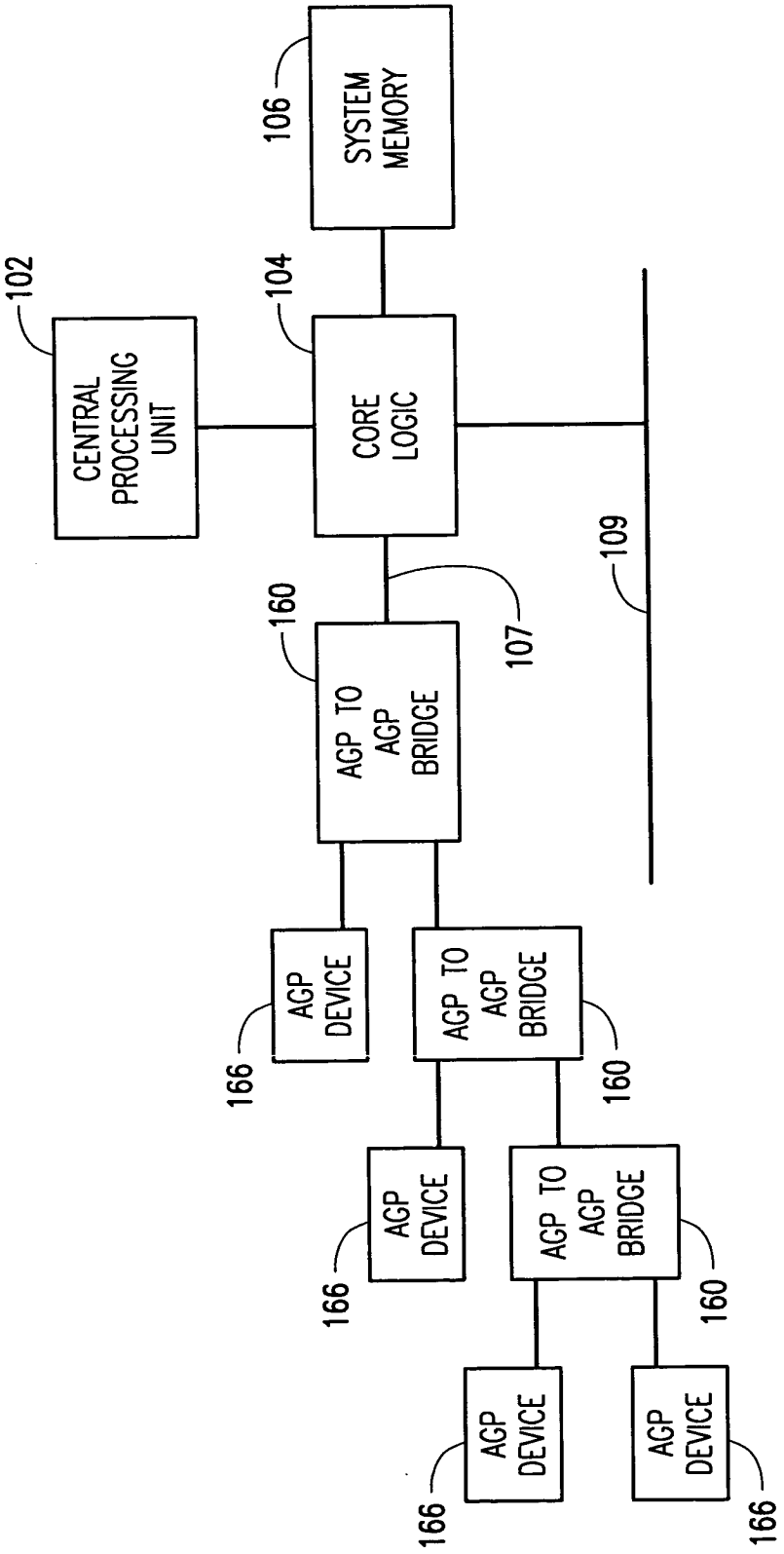

SYSTEM MEMORY
106
CENTRAL PROCESSING UNIT
102
CORE LOGIC
104
109
AGP TO AGP BRIDGE
160
107
AGP DEVICE
166
AGP TO AGP BRIDGE
160
AGP DEVICE
166
AGP TO AGP BRIDGE
160
AGP DEVICE
166
AGP DEVICE
166

FIGURE 16

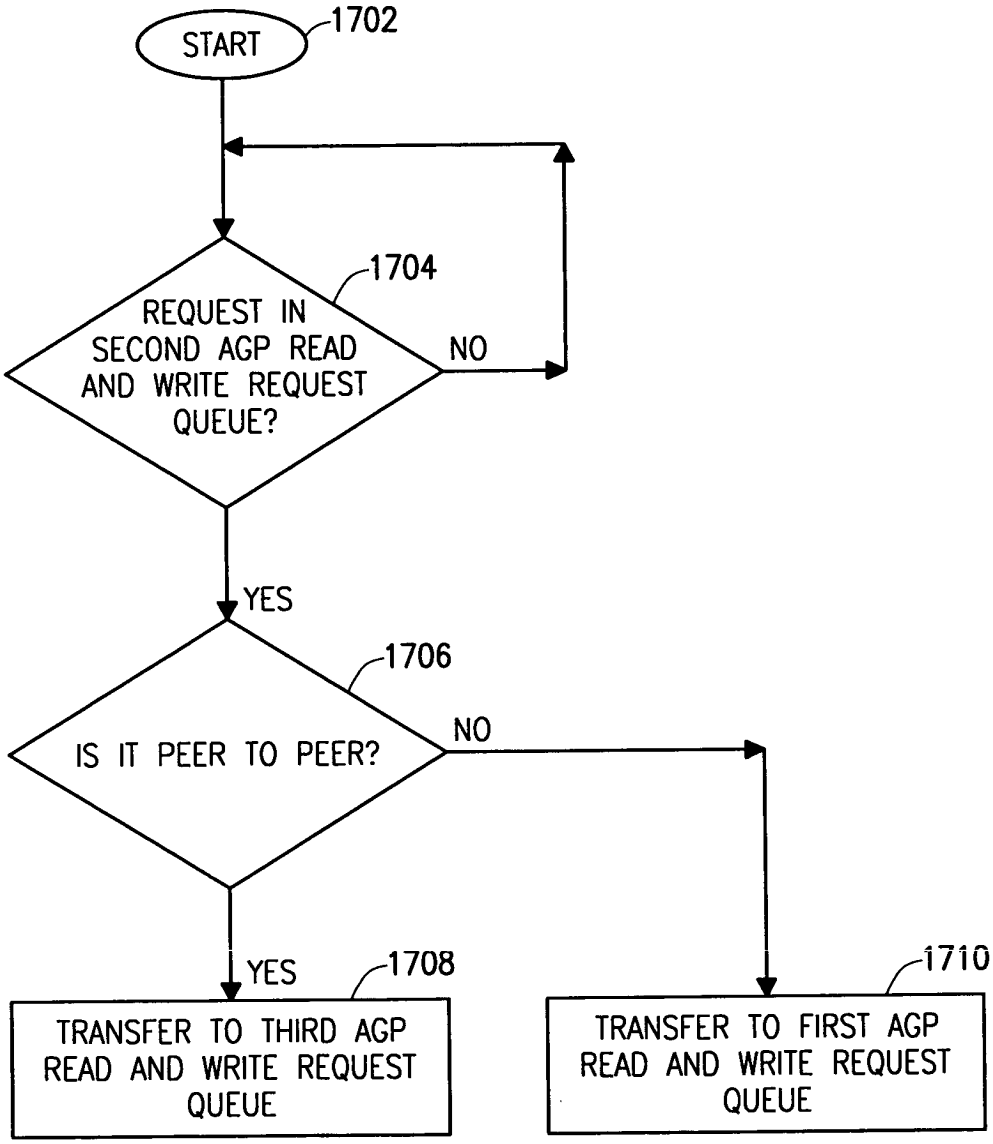

START
1702
1704
REQUEST IN SECOND AGP READ AND WRITE REQUEST QUEUE?
NO
YES
1706
IS IT PEER TO PEER?
NO
YES
1708
TRANSFER TO THIRD AGP READ AND WRITE REQUEST QUEUE
1710
TRANSFER TO FIRST AGP READ AND WRITE REQUEST QUEUE

FIGURE 17

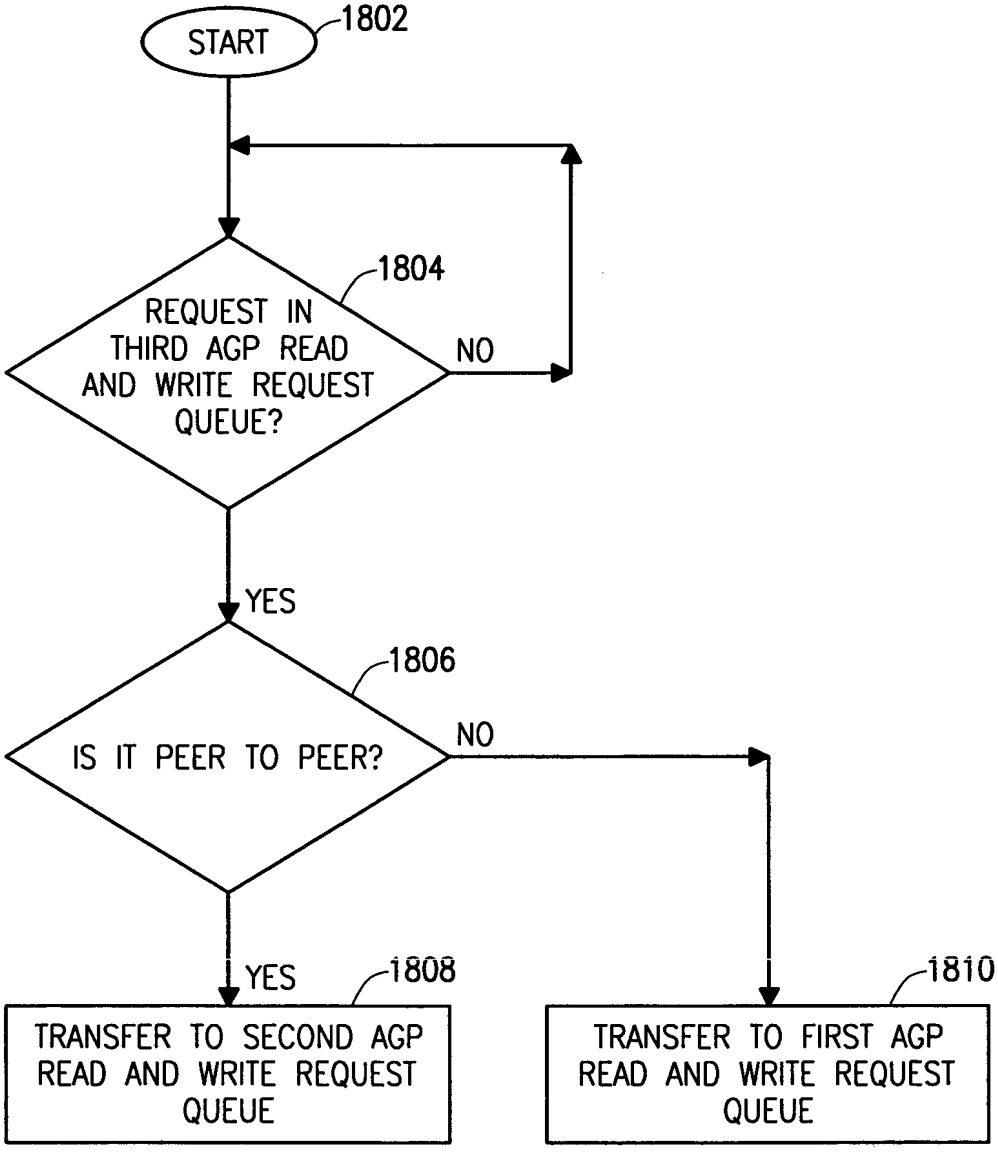

START
1802
1804
REQUEST IN THIRD AGP READ AND WRITE REQUEST QUEUE?
NO
YES
1806
IS IT PEER TO PEER?
NO
YES
1808
TRANSFER TO SECOND AGP READ AND WRITE REQUEST QUEUE
1810
TRANSFER TO FIRST AGP READ AND WRITE REQUEST QUEUE

FIGURE 18

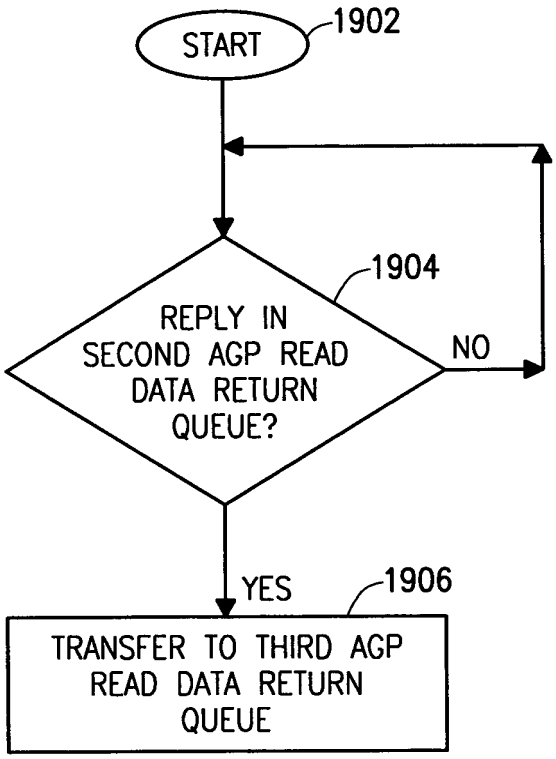


FIGURE 19

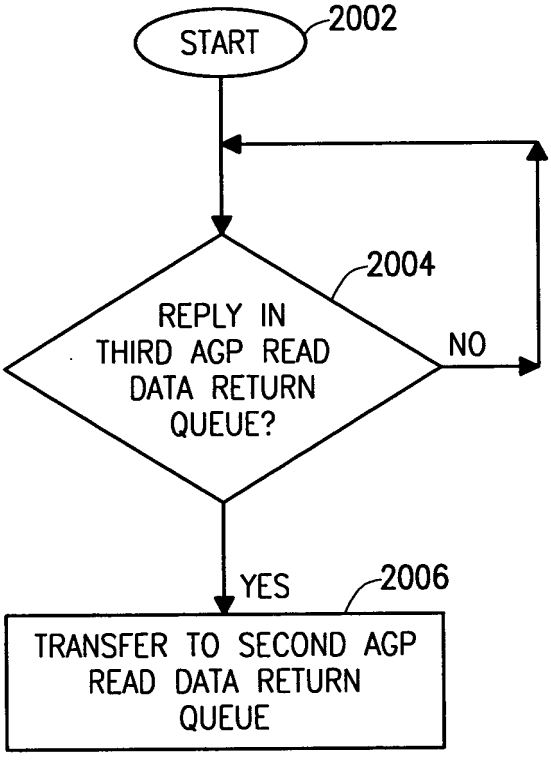


FIGURE 20

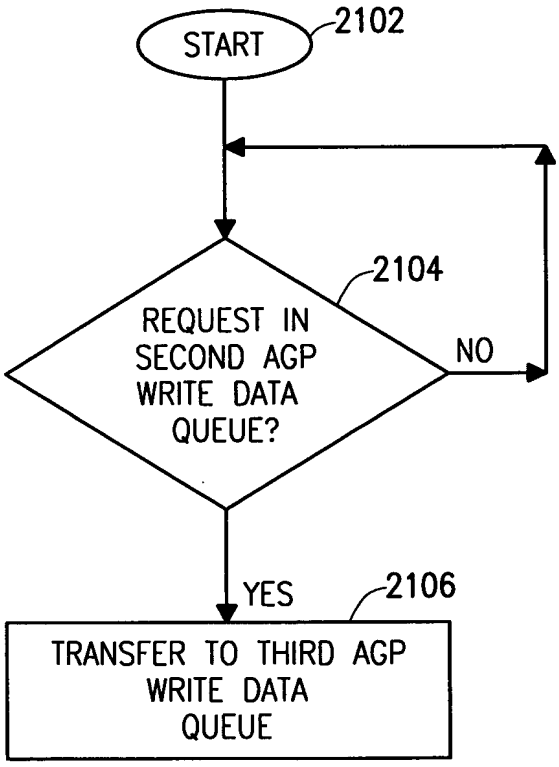


FIGURE 21

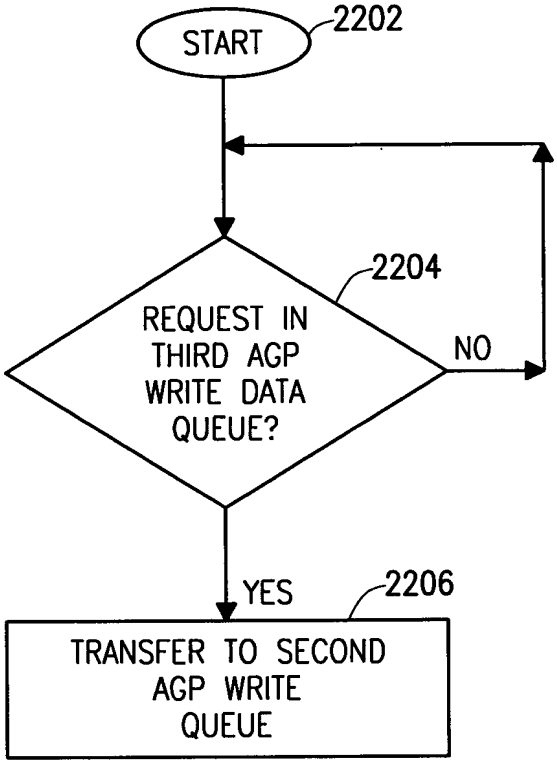


FIGURE 22